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[VLSI - Lecture 6a: Interconnect \(Capacitance\)](#)

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[A Day in the Life of a SoC Hardware Engineer](#)

A Day in the Life of a SoC Hardware Engineer von Teresa Meng vor 2 Jahren 3 Minuten, 23 Sekunden 203.312 Aufrufe Thanks for watching. This is a typical day of my life as a hardware engineer and I had so much fun vlogging it ☺☺ Please give this ...

[FPGA Interview Questions Part 1](#)

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ESD (Part - 1) von Analog Layout \u0026 Design vor 1 Jahr 14 Minuten, 28 Sekunden 11.126 Aufrufe I/O ESD \u0026 LATCHUP go together. I will cover all these in multiple videos. This is part 1.

[Virtuoso - Part 1 - Schematic Capture using Virtuoso Layout](#)

Virtuoso - Part 1 - Schematic Capture using Virtuoso Layout von Tom Briggs vor 2 Jahren 17 Minuten 1.248 Aufrufe Introduces virtuoso and the schematic capture of a full-adder using , digital , logic gates and a NAND2 gate using , CMOS , transistors.

[} VLSI } 20 } Interconnects }](#)

} VLSI } 20 } Interconnects } von LEPROFESSEUR vor 7 Monaten 32 Minuten 321 Aufrufe Interconnects are very important, almost 70 percent , chip , area is consumed by interconnects. Interconnects increases , circuit , ...

[VLSI - Lecture 5d: Current and Future Trends](#)

VLSI - Lecture 5d: Current and Future Trends von Adi Teman vor 7 Monaten 14 Minuten, 10 Sekunden 812 Aufrufe Bar-Ilan University 83-313: , Digital , Integrated Circuits This is the fourth and final short section of Lecture 5 of the , Digital , Integrated ...

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